Scanning Probe Nanolithography for Fabrication of Si Quantum Device

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1. Introduction

A silicon quantum functional device based on nanostructures is one of promising candidates for future VLSIs. Especially, an Si nanowire with a nanometric quantum island between tunnel junctions, is suitable for single electron transistors (SETs) due to their low power consumption and quantum phenomena such as quantization of electric conductance [1-3].

We have applied an scanning probe nanolithography (SPNL) based on field-enhanced anodization to the surface of a silicon -on-insulator (SOI) wafer with octadecylsilyl (ODS) monolayer [4], for fabricating a silicon nanowire composed of a nanometric island between tunnel junctions in SETs. This paper describes the novel structure of an Si nanowire with a nanometric island between tunnel junctions fabricated by SPNL using single- and multi-probes. Electrical characteristics of SET developed by SPNL were also studied.

2. Experimental Procedure

Figure 1 shows the process flow of SPNL using the ODS monolayer. The SPNL draws nanometric SiO2 lines on the ODS monolayer vaporized on a 2 nm-thick thermal oxidized SOI wafer. The ODS monolayer is degraded by the electrochemical reaction induced in the absorbed water on the sample, and then surface Si molecules in the ODS are anodized. Using the ODS and SiO2 layers as multi-layered masks for wet etching with BHF and TMAT, respectively, a nanometric groove is formed at the surface Si layer of SOI.

Placing two tunnel junctions in series can form a simple SET in Fig. 2. Two tunnel junctions create a nanometric island where electrons can enter by tunneling through one of insulators. The transistor has three terminals like an ordinary field effect transistor; the outside terminal of each tunnel junction, and a gate terminal, which is capacitively coupled to the island between two tunnel junctions. Figure 3 shows the fabrication process of the Si nanowire with a nanometric island between tunnel junctions.

SEM photographs of multi-probes array fabricated by the LOCOS (local oxidation of silicon) technique [5,6] are shown in Fig. 4(a). The SPNL using the multi-probes can pattern in parallel on an Si surface coated by ODS monolayer, leading to high throughput in the nanolithography. The commercial laser detection system is attached on the imaging probe. When approaching the imaging probe to a surface of sample under controlling the vertical deflection of the probe using the laser system, the lithography probes array settled in right or left sides surely contacts on the surface in Fig. 4(b). Figure 5 shows a photograph of multi-probes array approaching a SOI surface with two alignment pads for the imaging probe and four source-drain pads for the multi-probes.

3. Results and discussions

AFM images in Fig. 6 exhibit nanometric SiO2 lines and grid patterns drawn by SPNL using a single-probe on ODS/SiO2/SOI wafer. Nanometric grooves after development by wet and dry etchings are also illustrated in Fig. 6. The height of SiO2 lines reaches about 1.5 nm on the wafer, and the nanometric grooves with a width of 80 nm and a depth of 50 nm are formed at the surface Si layer of SOI after wet etching.

AFM images in Fig. 7 show SiO2 lines patterned by the multi-probes at alignment pads and at four source-drain pads. Each line is about 100 nm in width and 2 nm in height, which is sufficient size as a mask pattern for nanometric wet etching. The parallel SPNL is thought to be useful as a nanofabrication technique with high throughput.

SEM photographs and AFM images of Si nanowires including a nanometric island between two tunnel junctions are shown in Fig. 8. The nanometric islands were shaped a tetragonal pyramid with a base about 40 nm squares.

Figure 9 exhibits examples of the \( I_g-V_g \) characteristics at temperature ranging from 4 K to 100 K at a vacuum less than 1 \( \times 10^{-7} \) Pa. Here, the drain voltage was changed from 1 mV to 5 mV. Large Coulomb blockade oscillations are observed in the SET at 4 K. The number of current peaks is four, and the peak current increases rapidly with an increase of the gate voltage above 2.4 V. At higher gate voltages, electrons penetrate the lower tunneling barriers. The similar trend of Coulomb blockade oscillations is observed at 20 K, but the number of current peaks above 50 K is only one. The SET has a narrow range of the gate voltage for its operation at lower temperature.

4. Conclusion

This paper reported novel fabrication process of silicon nanowire with a nanometric island between tunnel junctions for SET using SPNL technique with ODS monolayer. The multi-probes SPNL is also proposed for improvement of throughput in nano-fabrication process. The 40 nm-wide and 80 nm-thick Si nanowire including a 40 nm-squares island was entirely accomplished on a silicon-on-insulator wafer using a single-probe. The Si island was located between two tunnel junctions at the center of the wire. Coulomb blockade oscillations were clearly observed below 50 K in the \( I_g-V_g \) characteristics of the SET fabricated by SPNL and LOCOS process. The SPNL with the self-assembled monolayer was effective technique for fabrication of a SET.

References

Fig. 1 Fabrication process of scanning probe nanolithography with self-assembled monolayer.

Fig. 2 Si nanowire with quantum island between tunnel junctions for operating SET.

Fig. 3 Fabrication process of Si nanowire with quantum island for simple SET.

Fig. 4 Multi-probes array fabricated by LOCOS technique.

Fig. 5 Photograph of multi-probes array on SOI surface.

Fig. 6 AFM images of SiO₂ lines and grooves fabricated by SPNL using single-probe.

Fig. 7 AFM images of anodized lines by multi-probes.

Fig. 8 SEM photographs and AFM images of SET.

Fig. 9 \( I_d - V_g \) characteristics of SET at temperature ranging from 4 K to 100 K at a high vacuum.