Shot Number Estimation for EB Direct Writing for Logic LSI Utilizing Character-Build Standard-Cell Layout Technique

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ABSTRACT

Electron Beam direct writing (EBDW) technology is the most cost-effective lithography tool for small-volume logic-LSI fabrication. The EB exposure time will be greatly reduced by applying character-projection (CP) aperture. But the applicable number of CP aperture is limited to 25-400 depending upon EB lithography apparatus. The cell-based logic LSIs are composed of standard-cells (SCs) whose number is 400-1000. Therefore, it is impossible to implement all SCs as CP apertures, because the SCs are placed to 4-directions in general.

We had proposed the new technique named “Character-Build (CB) standard-cell”, and demonstrate the most of the combination-logic SCs can be composed by only 17 CP apertures. In this paper, not only combination-logic SCs but also sequential-logic SCs are considered. The number of EB-shots and the chip-area are estimated for some sample circuits.

Compared to the simply-limited SCs, The EB shot number is 30-40% reduced by using proposed CB standard-cell, when the CP aperture numbers are 20-30. Moreover, CB standard-cell was advantageous in the module area. Considering 2-directional placement of SCs, the combination of the EB apparatus with 50-100 CP apertures and the CB standard-cell technique may be the best method for high-speed EB direct-writing.

Keywords: EB direct write, Mask layout, Standard cell, Character projection, Cell projection, Block exposure

1. INTRODUCTION

The cost of a photo-mask is becoming very expensive with the progress of LSI process-technology. A mask-set for 90nm process technology costs more than one million dollar. On the other hand, the kinds of application-specific logic LSI for various digital devices, such as mobile-phone, digital-still camera, and DVD recorder, are increasing. Therefore, mask reduction becomes the serious problem, especially for the small-volume production LSIs.

Electron-beam direct-writing (EBDW) is a good lithography tool for small-volume production LSIs, because the layout pattern can be delineated without photo-mask. The throughput of EBDW is, however, much lower than that of a photo-lithography. The layout pattern is divided into small rectangles, which can be exposed by one shot, in the EBDW system. EBDW time is proportional to the shot number, which is calculated by the number of total figures divided by the rectangle exposed by one shot. The shot number is greatly increased with the progress of integrated device density. In the character-projection (CP) EB exposure system, multiple rectangles can be exposed by one shot by using stencil masks, which is named by CP aperture. The EB exposure time is dramatically decreased, by employing frequently referenced patterns to the character aperture.

The number of CP apertures is limited to 25-400 depending upon CP-EB exposure system. Increase of the number of CP aperture is difficult, because the settling time (overhead time for single shot) will be increased. Therefore, the selection of the most frequently used patterns is important. The memory cell layout and the peripheral circuit layout, such as the decoder and the sense-amplifier, has been the good candidate for the character aperture. The standard-cell layout is also the good candidate, because the cell-height of standard-cells(SCs) get smaller than 5 μm below the 130
nm process. The kinds of SCs are several hundreds, and the selection of frequently used SCs is essential. The selection method of SCs and the throughput enhancement demonstration were studied in 2000[4].

The logic-synthesis using simply-limited SCs has disadvantage in the target-frequency and reference-cell-number. Figure 1 shows the logic-synthesized results of DES encryption circuit module from OPENCORES.ORG[5] using normal and simply-limited SCs. The SCs library is supplied from academia[6], and the process technology is 0.35 μm CMOS. Logic synthesis is carried out by synopsys “Design-Compiler”. The referenced-cell number is increased by about 80% for logic-synthesis using 25 SCs. The increase of referenced-cell number results in the increase of EB shots, if the cell is exposed by one shot. The logic synthesis for the high-speed operating frequency was failed. It means that the speed performance is degraded by the synthesis of limited SCs. It was also reported[4] that there is some disadvantage in chip-area by using simply-limited SCs.

![Figure 1](image_url)  
Figure 1. The increase of reference-cell number and the speed degradation in the sample circuit synthesized by the limited SCs.

## 2. CHARACTER-BUILD STANDARD-CELL LAYOUT TECHNIQUE AND 2-DIRECTIONAL CELL PLACEMENT

### 2.1. Character-Build Standard-Cell

We have proposed the new preparation method of standard-cells (SCs) library named “Character-Build standard cell” in PMJ 2005[7]. The various kinds of SCs can be composed by the combination of CP apertures. The most of 223 standard cells (combination-logic SCs) can be composed by only 17 CP apertures using this technique. Figure 2 shows the example of Character-Build standard cells. AND cell, complex-function gate cell, and input-inverted cell are composed by the combination of primitive gate such as NAND, NOR and Inverter.

The simple combination of primitive gate has disadvantage in area, then the novel “additive” cell is introduced. This “additive” cell is used as the inverter, which is the attachment of “basic” cell. The layout example of “additive” cell is shown in Fig.3. The NOR primitive gate combined with inverter compose OR function as shown in Fig.3(a). But the size of this cell is larger than the optimized OR cell as shown in Fig.3(a). In order to recover this problem, the “additive” inverter layout is prepared in addition to the normal inverter. The right end of the NOR “basic” cell is terminated by source wiring to Vdd and Gnd, and the left end of “additive” cell is also terminated by the source wiring. The source
wiring layout pattern is shared between “basic” cell and “additive” cell. Therefore the cell size composed of “basic” cell and “additive” cell is 1 unit smaller than the cell composed of two “basic” cells. This technique is called “source sharing”, and his technique is used for other “additive” cells such as 2X powered inverter and 4X powered inverter.

<table>
<thead>
<tr>
<th>NORMAL-Cell</th>
<th>CB-Cell</th>
<th>CP-Shot</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="NOR (basic)" /></td>
<td><img src="image" alt="Inverter (basic)" /></td>
<td>2</td>
</tr>
<tr>
<td><img src="image" alt="NOR (basic)" /></td>
<td><img src="image" alt="NOR (basic)" /></td>
<td>3</td>
</tr>
<tr>
<td><img src="image" alt="NOR (basic)" /></td>
<td><img src="image" alt="Inverter (additive)" /></td>
<td>2</td>
</tr>
</tbody>
</table>

Figure 2. Example for composed standard-cells by Character-Build technique. Original standard-cell is exposed by multiple CP shots.

Figure 3. Layout pattern of OR cell using “source sharing”.

![Source Sharing](image)
2.2 The Selection of minimum Characters

It was announced the most of the combination-logic SCs can be exposed by only 17 cell characters. In order to synthesize sequential-logic circuit from verilog-HDL code, some kinds of Flip-Flop SCs are necessary. In order to select Flip-Flop, The sample circuit written in verilog-HDL code from OPENCORES.ORG\(^5\) is used, and the logic-synthesis is carried out by synopsys "Design Complier."

In the experimental result of logic-synthesis, the most referenced Flip-Flop is "D Flip-Flop", and the next is "D Flip-Flop with Reset". The 3rd one is "D Flip-Flop output inverted", but the referenced number is very small. "D Flip-Flop with Reset" can be taken the place of "D Flip-Flop", however, reference frequency of "D Flip-Flop" is overwhelming, compared to the reference frequency of "D Flip-Flop with Reset". Therefore "D Flip-Flop" is remained as the primitive SCs. "D Flip-Flop output inverted" is substituted by the combination of "D Flip-Flop" and "inverter". As a result, "D Flip-Flop" and "D Flip-Flop with Reset" are added to 17 CP apertures as shown at the right part of Fig.4. 150 kinds of standard-cells can be generated from 19 CP apertures.

![Figure 4. The number of standard-cells which can be composed by CP apertures.](image)

The selection strategies of SCs more than 19 are described here. The referenced standard-cell with high reference frequency is added from the synthesized result. For example, Exclusive-OR (EXOR) gate is composed from the combination of NOR and AOI gates in the case of using 19 CP apertures as shown in Fig.5 (a). If the reference frequency of EXOR is high, and more CP apertures are permitted, EXOR gate is registered to the CP aperture, as shown in Fig.5 (b). The total EB shots decreases, because the EB shot for single EXOR gate decreases from 2 to 1.

![Figure 5. The EXOR cell composed from (a) two characters and (b) one character.](image)

In addition to EXOR cell, these are some SCs with high reference frequency as shown in Fig.6. The SCs in Fig. 6 (a), can be registered to CP aperture, however, The SC in Fig. 6 (b) can not be registered to CP aperture, because, the cell size is larger than the maximum size of CP aperture.
2.4. 2-directional Standard-Cell Placement

In the normal place-and-route (P&R) layout procedure, SCs pattern are placed to four-direction (NORMAL, X-MIRROR, Y-MIRROR, and XY-MIRROR). It means that the 4 X CP aperture is necessary to use one character. In order to reduce the necessary number of CP apertures, the experimental layout, in which SCs arrangement of 2 or 4 directions are forbidden, was performed. Figure 7 shows the layout results for the bus-control-module in microprocessor. The P&R is carried out by synopsys “Astro”. The area size is equal for 2-directional (a) and 4-directional (b) placement, and the increase of wire length is as small as 0.2%. In the 1-directional (c) placement, the area size increases 2 times the original layout, because there is vacant area between Vdd and Gnd wiring. As a result, 2-directional placement should be applied for the reduction of the number of CP apertures.
3. VERIFICATION OF CHARACTER-BUILD STANDARD-CELL LAYOUT TECHNIQUE

3.1 EB Shots Number

In the normal standard-cell, the number of EB shot is equal to the total referenced number of standard-cell, because a single standard-cell can be delineated by a single EB shot. In the proposed CB standard-cell, the EB shot number is calculated by the following equation, because a single standard-cell is exposed by multiple CP shots. For example, \( CP_{shot \_for \_Cell} \) for EXOR gate in Fig.5(a) is 2, and \( CP_{shot \_for \_Cell} \) for EXOR gate in Fig.5(b) is 1.

\[
EB\_Shot = \sum_{referred \_cell} (Cell\_reference\_number \times CP_{shot \_for \_Cell})
\]

Some experimental logic-synthesis were carried out using normal-SCs and CB-SCs library, by using sample verilog-HDL design from OPENCORES.ORG. The number of usable CP apertures are 19, 25, 50, and 150. In the normal-SCs library, the number of usable SCs is equal to that of usable CP apertures. In the CB-SCs library, the number of usable SCs is much larger than that of CP apertures, as illustrated in Fig.4. Total EB-shots number was calculated from 4 synthesized designs, based on the above-mentioned equation, as shown in Fig.8.

![Figure 8](image)

Figure 8. Estimated EB shot number using the normal and the CB Standard-cells.

The total EB-shots decreases with increasing CP apertures. The reduced amount of EB shots for CB-SCs is much larger than that of normal SCs, when the number of CP apertures is varied from 19 to 25. This data is the proof of the advantage of CB-SCs. On the other hand, EB shot number for CB-SCs is the same or smaller than that of normal SCs, when the number of CP apertures is more than 50 to 100. This is explained by Fig. 9, in which the cell-reference numbers for each cells by the normal logic-synthesis with full SCs are shown. If the number of CP apertures exceeds 50, almost all necessary SCs can be registered. Therefore, CB-SCs technique is not effective, when the number of applicable CP apertures is larger than that of the used standard cells.
3.2 Chip Area Penalty

In addition to EB shots number, chip-area-penalty was verified. It is calculated on the same condition as EB-shots-number calculation. Additionally, the condition of “COMBINED Standard-Cell” was added. This cell is considered as the CB standard cells without additive cells using the “source-sharing” technique.

Chip-area-penalty of using CB Standard-Cell is shown by the next expression, and the calculated results are shown in Fig.10.
\[
\text{AREA\_Penalty} = BC \times \sum_{\text{referenced\_cell}} (\text{CPshot\_for\_Cell} - \text{CPshot\_for\_Cell}_{\text{Additive\_Character}} - 1)
\]

CB Standard-Cell is effective in Chip-area-penalty as the result as well as EB-shots-number. And, additive-character with “source-sharing” technique contributes to the chip area reduction.

4. CONCLUSION

EB shot number is 30-40% reduced by using proposed CB standard-cell, when the CP apertures numbers are 20-30. Moreover, CB standard-cell was advantageous in the module area compared with reduced normal standard-cell. Then, the number of CP aperture should be limited in order to decrease the settling time. The area penalty in 2-directional P&R is 0.05 % in the sample layout. Therefore, character-build SCs with 20-30 CP apertures (40-60 CP apertures for 2-directional placement) may be the best method for logic layout. Considering that the embedded memory must be exposed by CP apertures, 80-100 CP apertures may be the best solution for high-speed EBDW.

Other than our work, some design methodologies for EBDW throughput-enhancement are studied in 2005[8] and 2006[9]. The EB throughput enhancement can be realized by some restriction of layout design, with little area-penalty and performance-penalty. We believe that EBDW with these design methodologies is the promising technology for small-volume production LSIs.

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REFERENCES